Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	46390	ferroelectric	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/09/21 09:02
L2	11290	1 same capacitor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/09/21 09:02
L3	4225	(438/238,239,253,397).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/09/21 09:03
L4	579	3 and capacitor and 1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2005/09/21 09:34
L5	519	2 and 3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2005/09/21 09:39
L6	11259419	@ad<"20000920" or @rlad<"20000920"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2005/09/21 09:20
L7	317	4 and 6	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2005/09/21 09:33
L8	2551	(438/3,240).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/09/21 09:34
L9	1102	8 and capacitor and 1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2005/09/21 09:35
L10	797	9 not 4	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2005/09/21 09:37
L11	413	10 and 6	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	ADJ	ON	2005/09/21 09:39

L12	519	2 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/09/21 09:40
L13	0	5 not 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/09/21 09:40
L14	1	dummey electrode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/09/21 09:43
L15	3	dummey with electrode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/09/21 09:45
L16	2058	2 and (second adj2 electrode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/09/21 09:46
L17	6094	3 or 8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/09/21 09:46
L18	424	16 and 17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/09/21 09:46
L19	231	18 and 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/09/21 09:47
L20	119	19 not 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/09/21 10:42
L21	64	Chain FRAM	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2005/09/21 10:43

IEEE *Xplore* ©
RELEASE 2.1

▮▯▮Search Results

BROWSE   SEARCH   IEEE XPLORE GUIDE

Results for "((chain fram)<in>metadata)"   ✉e-mail
Your search matched **5** of **1237766** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History   **Modify Search**

New Search   ┌─────────────────────────────────┐ ┌──┐
                                         │ ((chain fram)<in>metadata)   │ │≫ │
                                         └─────────────────────────────────┘ └──┘

                                         ☐ Check to search only within this results set

» Key   **Display Format:**   ◉ Citation   ○ Citation & Abstract

         📱 Indicates full text access

IEEE JNL IEEE Journal or   **Select   Article Information**
              Magazine

IEE JNL   IEE Journal or Magazine   ☐   1. **A sub-40-ns chain FRAM architecture with 7-ns cell-plate-line drive**
                                                Takashima, D.; Shuto, S.; Kunishima, I.; Takenaka, H.; Oowaki, Y.; Tanaka, S.
IEEE CNF IEEE Conference   Solid-State Circuits, IEEE Journal of
              Proceeding   Volume 34, Issue 11, Nov. 1999 Page(s):1557 - 1563
                                                Digital Object Identifier 10.1109/4.799863
IEE CNF   IEE Conference
              Proceeding   Abstract | Full Text: PDF(340 KB)   **IEEE JNL**

IEEE STD IEEE Standard
                                         ☐   2. **High-density chain ferroelectric random access memory (chain FRAM)**
                                                Takashima, D.; Kunishima, I.;
                                                Solid-State Circuits, IEEE Journal of
                                                Volume 33, Issue 5, May 1998 Page(s):787 - 792
                                                Digital Object Identifier 10.1109/4.668994

                                                Abstract | Full Text: PDF(140 KB)   **IEEE JNL**

                                         ☐   3. **A sub-40 ns random-access chain FRAM architecture with a 768 cell-plate**
                                                Takashima, D.; Shuto, S.; Kunishima, I.; Takenaka, H.; Oowaki, Y.; Tanaka, S.
                                                Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 199
                                                International
                                                15-17 Feb. 1999 Page(s):102 - 103
                                                Digital Object Identifier 10.1109/ISSCC.1999.759147

                                                Abstract | Full Text: PDF(300 KB)   **IEEE CNF**

                                         ☐   4. **Gain cell block architecture for gigabit-scale chain ferroelectric RAM**
                                                Takashima, D.; Oowaki, Y.; Kunishima, I.;
                                                VLSI Circuits, 1999. Digest of Technical Papers. 1999 Symposium on
                                                17-19 June 1999 Page(s):103 - 104
                                                Digital Object Identifier 10.1109/VLSIC.1999.797251

                                                Abstract | Full Text: PDF(200 KB)   **IEEE CNF**

                                         ☐   5. **A 76-mm^2 8-Mb chain ferroelectric memory**
                                                Takashima, D.; Takeuchi, Y.; Miyakawa, T.; Itoh, Y.; Ogiwara, R.; Kamoshida,
                                                Doumae, S.M.; Ozaki, T.; Kanaya, H.; Yamakawa, K.; Kunishima, I.; Oowaki, Y
                                                Solid-State Circuits, IEEE Journal of
                                                Volume 36, Issue 11, Nov. 2001 Page(s):1713 - 1720
                                                Digital Object Identifier 10.1109/4.962293

                                                Abstract | Full Text: PDF(329 KB)   **IEEE JNL**